# Computer Architecture

# Lab Sheet 2 – Logic Circuits 2

**Jack Carroll**

**T00194823**

**Materials:** Logic Box, Gates – AND, NAND, OR, Inverter and NOR gate,wire

**Method for Circuit 1:**

1. Build Circuit 1 as shown in Figure 1.
2. Connect the inputs to the switches on the logic box as categorized in Figure 1.
3. Connect the output to the LED (Light Emitting Diode).
4. Write in the truth table results for Figure 1.

**Report:**



*Figure 1*

|  |  |
| --- | --- |
| **S3 S2 S1 S0** | **LED** |
| 0 0 0 0 | 1 |
| 0 0 0 1 | 0 |
| 0 0 1 0 | 0 |
| 0 0 1 1 | 0 |
| 0 1 0 0 | 0 |
| 0 1 0 1 | 0 |
| 0 1 1 0 | 0 |
| 0 1 1 1 | 0 |
| 1 0 0 0 | 0 |
| 1 0 0 1 | 0 |
| 1 0 1 0 | 0 |
| 1 0 1 1 | 0 |
| 1 1 0 0 | 0 |
| 1 1 0 1 | 0 |
| 1 1 1 0 | 0 |
| 1 1 1 1 | 0 |

*Lab Table 1 – Circuit 1*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S3 S2 S1 S0** | **LED** |  |  | *.* |
| 0 0 0 0 | 1 | 1 | 1 | 1 |
| 0 0 0 1 | 0 | 1 | 0 | 0 |
| 0 0 1 0 | 0 | 1 | 0 | 0 |
| 0 0 1 1 | 0 | 1 | 0 | 0 |
| 0 1 0 0 | 0 | 0 | 1 | 0 |
| 0 1 0 1 | 0 | 0 | 0 | 0 |
| 0 1 1 0 | 0 | 0 | 0 | 0 |
| 0 1 1 1 | 0 | 0 | 0 | 0 |
| 1 0 0 0 | 0 | 0 | 1 | 0 |
| 1 0 0 1 | 0 | 0 | 0 | 0 |
| 1 0 1 0 | 0 | 0 | 0 | 0 |
| 1 0 1 1 | 0 | 0 | 0 | 0 |
| 1 1 0 0 | 0 | 0 | 1 | 0 |
| 1 1 0 1 | 0 | 0 | 0 | 0 |
| 1 1 1 0 | 0 | 0 | 0 | 0 |
| 1 1 1 1 | 0 | 0 | 1 | 0 |

*Theory Table 1 with Lab Result (LED) – Circuit 1*

Conclusion: In the lab table, the results indicate that the circuit is a NOR Gate because when all 0s are present, the output takes a 1. Other than that, the output takes in a 0 when any input of 1 is featured in the circuit.

Similarly, the theory table displays the same outputs as the lab table suggests showing that the circuit seems to be a NOR gate due to the reasons explained in the lab table’s conclusion. When the two NOR sums were calculated, the answers to these were interpreted through the AND gate which leads to the NOR gate being created from the outputs.

**Method for Circuit 2:**

1. Build Circuit 2 as shown in Figure 2.
2. Connect the inputs to the switches on the logic box as categorized in Figure 2.
3. Connect the output to the LED (Light Emitting Diode).
4. Write in the truth table results for Figure 2.

**Report:**



*Figure 2*

|  |  |
| --- | --- |
| **S3 S2 S1 S0** | **LED** |
| 0 0 0 0 | 1 |
| 0 0 0 1 | 1 |
| 0 0 1 0 | 1 |
| 0 0 1 1 | 1 |
| 0 1 0 0 | 1 |
| 0 1 0 1 | 1 |
| 0 1 1 0 | 1 |
| 0 1 1 1 | 0 |
| 1 0 0 0 | 1 |
| 1 0 0 1 | 1 |
| 1 0 1 0 | 1 |
| 1 0 1 1 | 1 |
| 1 1 0 0 | 1 |
| 1 1 0 1 | 1 |
| 1 1 1 0 | 1 |
| 1 1 1 1 | 1 |

*Lab Table 2 – Circuit 2*

|  |  |  |  |
| --- | --- | --- | --- |
| **S3 S2 S1 S0** | **LED** |  | *+ S3 (Z)* |
| 0 0 0 0 | 1 | 1 | 1 |
| 0 0 0 1 | 1 | 1 | 1 |
| 0 0 1 0 | 1 | 1 | 1 |
| 0 0 1 1 | 1 | 1 | 1 |
| 0 1 0 0 | 1 | 1 | 1 |
| 0 1 0 1 | 1 | 1 | 1 |
| 0 1 1 0 | 1 | 1 | 1 |
| 0 1 1 1 | 0 | 0 | 0 |
| 1 0 0 0 | 1 | 1 | 1 |
| 1 0 0 1 | 1 | 1 | 1 |
| 1 0 1 0 | 1 | 1 | 1 |
| 1 0 1 1 | 1 | 1 | 1 |
| 1 1 0 0 | 1 | 1 | 1 |
| 1 1 0 1 | 1 | 1 | 1 |
| 1 1 1 0 | 1 | 1 | 1 |
| 1 1 1 1 | 1 | 0 | 0 |

*Theory Table 2 with Lab Result(L)– Circuit 2*

Conclusion: The lab table shows that the LED result does not signify a specific gate according to the inputs. But due to the odd 0 output in the input 0111, the output raises some questions about what gate is taking effect here. In the 0111 input, a 0 output is given since S3 which is 0 has a low input while the other inputs feature a high input. It is possible that a NAND gate is in effect as S2, S1 and S0’s 3 inputs take a 0 when the input is high leading to the output taking a 1.

The theory table matches the lab table where there is a 0 output taken in the 0111 input due to the reasons specified in the lab table conclusion. Thus, this strengthens the fact that this table seems to contain a NAND gate in the 0111 input. Surprisingly, the rest of the table does not match the lab table as the 1111 input gave out a 1 output due to the presence of the OR gate in the end. The result matched the lab table result where the NAND sum of S2, S1 and S0 combined with S3 to form the OR gate which gave away a 1 input. Then, the NAND gate causes the S2, S1 and S0 (111) high input to give out a 0 output. The subsequent OR gate gave a 1 as the NAND gate OR S3 gave out a 1 when there is any 1 in the input. This proves that the circuits match each other with the NAND gate (1111) within the circuit.